

PROCESSORS

EnSilica's range of eSi-RISC soft processor cores is aimed at system-on-chip designs, writes **Steve Bush**

Soft chip cores for Asics and FPGAs

Chip design firm EnSilica has introduced three configurable and soft processor cores for Asics and FPGAs: eSi-1600, eSi-3200 and eSi-3250.

The cores are based on EnSilica's eSi-RISC scalable processor architecture, which supports 16-bit and 32-bit configurations, selectable Harvard/von Neumann memory, and configurable cache options.

"The highly pipelined nature of their design gives customers a solution that can be migrated between FPGA types or even to Asic technologies," says EnSilica.

Multiple choice

eSi-1600 is a 8,500-gate 16-bit processor that delivers up to 0.7Dmips/MHz.

Aimed at energy monitoring, intelligent sensors, medical use and wireless networking, power is 15µW/MHz on 0.13µm silicon.

eSi-3200 is a 32-bit core designed for use with on-chip memory. It has 15,000 gates and the five-stage pipeline can run at 700MHz on a 90nm process.

At 0.9Dmips/MHz, the core is aimed at applications requiring more code space than the eSi-1600 can provide, such as wireless communications and media processing, according to EnSilica.

eSi-3250 is optimised for off-chip memory and has configurable instruction and data caches (4-64kbyte, direct mapped or 2-way or 4-way associative).

"In this configuration, the core is still only 20,000 gates," claims the firm.

It can deliver 1.2Dmips/MHz, and there is an optional IEEE 754 floating point unit and MMU.

Intended applications are those with complex operating systems.

Tool choice

Internal company tools allow other configurations to be created, says EnSilica technical director Dr David Wheeler.

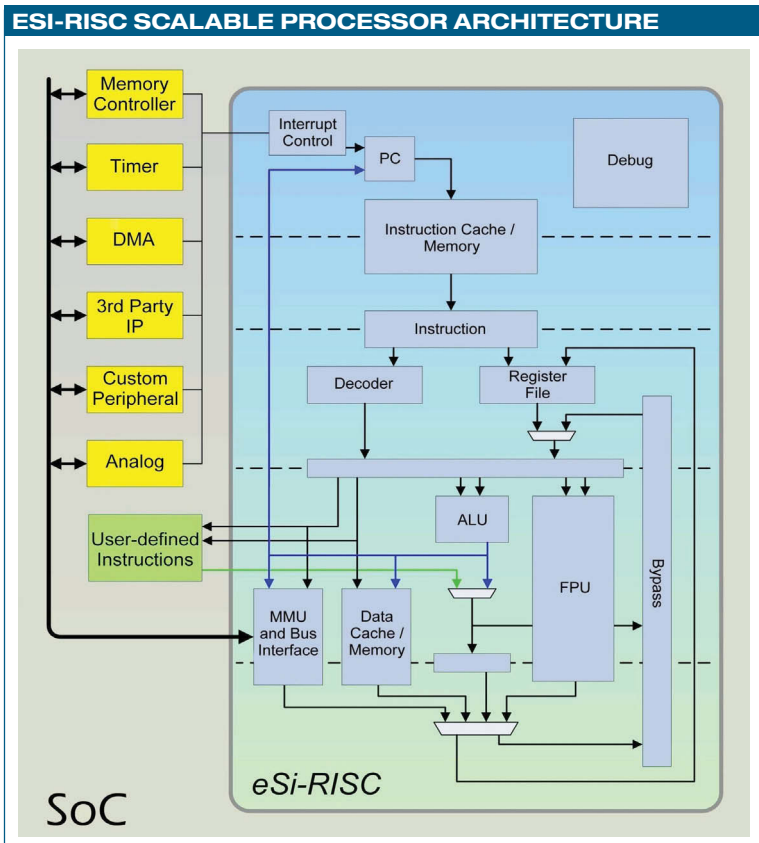
Customer software development tools, including C and C++ compilers, assembler and simulator, allow engineers to switch between cores to test implementation. They also allow options such as the multiplier and divider to be switched in and out to explore trade-offs.

"If you want more than the three basic cores, you can come back to us for, an extra instruction," says Wheeler. "We will implement it, and it will appear in the customer tools."

All cores have an instruction set that has a number of optional instructions and addressing modes, as well as support for up to 96 user-defined instructions.

"System clock speeds of above 200MHz can also be achieved in Altera Stratix IV and Xilinx Virtex-6 FPGAs," says EnSilica. "All processors use the industry-standard AMBA APB and AXI buses. We have a library of APB-based peripherals, including UART, SPI, I2C, timers and a 10/100 Ethernet MAC."

Development tools have been ported to the architecture to create a single development tool chain, including GCC 4.4.0, Binutils 2.20 and GDB 7.0 – all integrated into



the Eclipse 3.5 development environment.

"One of the most important things is that this is an industry-standard tool chain, based on Eclipse and GNU," says Wheeler. ●

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