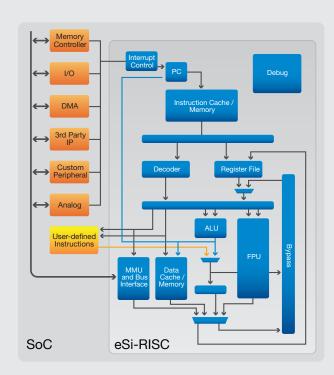




# eSi-RISC – Configurable Embedded Processor IP

eSi-RISC is a highly configurable microprocessor architecture for embedded systems, that scales across a wide range of applications. The core has been silicon proven in a number of ASIC and FPGA technologies.



### **Features**

- Configurable 16 or 32-bit, 5-stage pipelined RISC, load-store architecture.
- Implemented in as little as 8k ASIC gates for minimum 16-bit configuration.
- Intermixed 16 and 32-bit instructions gives exceptional code density.
- Uses industry standard bus architecture for IP interconnection (AMBA AXI/AHB/APB).
- Configurability and custom instructions will deliver a solution with exceptionally low-lower.

- Choice of von Neumann or Harvard memory architecture.
- Supports user and supervisor modes.
- JTAG or serial hardware debug.
- Applications include sensors, medical, power management, metering, wireless or mobile products.

### **Benefits**

- Highly configurable, allowing the processor to be tailored to fit a wide range of applications, on both FPGA and ASIC technology.
- Performance and code density amongst the very best available.
- Silicon proven.
- License-free SW development using GNU tools.
- · Competitive licensing terms.
- Backed up by the EnSilica reputation for quality design services.

### Scalability

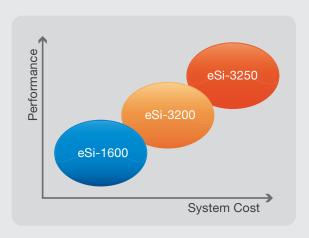
EnSilica have defined a family of processor cores that demonstrates the versatility of the eSi-RISC configurable architecture to cover a wide range of applications.

### eSi-1600

EnSilica's eSi-1600 16-bit CPU core is a low-cost, low-power processor. It offers similar performance to more expensive 32-bit CPUs while having a system cost comparable to that of 8-bit CPUs.

www.ensilica.com eSi-RISC IP Overview





### eSi-3200

EnSilica's eSi-3200 32-bit CPU core is particularly suited to embedded control applications.

### eSi-3250

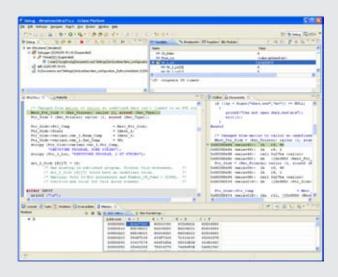
EnSilica's eSi-3250 32-bit CPU core is a high-performance processor ideal for integration into ASIC and/or FPGA designs with off-chip memories. The eSi-3250 is suited to a wide range of applications including running complex operating systems such Linux and uClinux.

### Development Kit

A hardware development kit is available for evaluating these cores. This board provides a range of memory and external interfaces to suit most applications.

# Toolchain

The toolchain is based upon the industry standard GNU toolchain, which includes an optimising C and C++ compiler, assembler, linker, debugger, simulator and binary utilities. All these tools can be driven by the customisable Eclipse IDE (Integrated Development Environment). The toolchain is available for both Windows and Linux hosts and is available to use at no additional cost.



## **IP Delivery**

The eSi-RISC is implemented as a soft IP core, based on synthesisable Verilog RTL and can be easily ported to a wide range of ASIC processes and FPGAs. The design is DFT ready, supporting full scan insertion for all flip flops and memory BIST.

A selection of AMBA peripherals are supplied with the core, including: UART, SPI, I2C™, Timer, PWM, Watchdog, GPIO, PS/2, Ethernet MAC as well as a static memory interface and DMA engine. By using an industry standard bus, a wide range of 3rd party IP cores can also be used.

# Support

By utilising EnSilica's system level design expertise to define the most appropriate configuration for your particular application and then using our design services to integrate the eSi-RISC core within your particular design, you can achieve a truly optimised solution without any of the pain often associated with embedded processor designs.

#### About EnSilica

EnSilica is an established company with many years' experience providing high quality frontend IC design services to customers undertaking FPGA and ASIC designs. We have an impressive record of success working across many market segments with particular expertise in multimedia

and communication applications. Our customers range from start-ups to blue-chip companies. EnSilica also offer a portfolio of IP, including a highly configurable 16/32 bit embedded processor called eSi-RISC and the eSi-Comms range of communications IP.

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