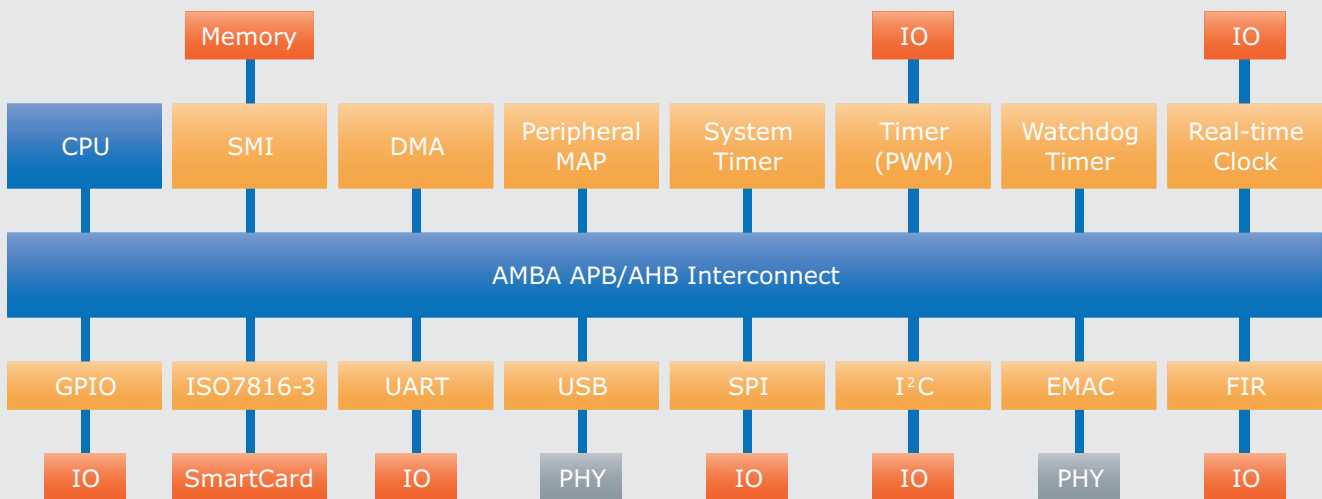


## eSi-Connect

EnSilica provide a comprehensive range of processor peripherals, each with a standard AMBA APB or AHB interface to simplify SoC integration and connectivity.

The eSi-Connect IP suite provides simple to integrate functions from widely used off-chip serial interfaces such as USB, I2C, SPI and UART to control functions including Timer, Real-time clock, Watchdog and GPIO. The blocks are configurable and provided with low-level software drivers suitable for real-time SoC deployment.



### eSi-I2C

The I2C slave and master is a 2 wire serial bus interface typically used to control peripherals requiring a low speed and limited control interface, for example an EEPROM. This module supports 100kbps and 400kbps I2C modes as well as 7 and 10-bit addressing and clock stretching.

### eSi-SPI

The eSi-SPI is a Serial Peripheral Interface (SPI). It uses a 4 wire serial bus to implement full-duplex, synchronous, serial communications. The block is software programmable and includes configurability for word size (8 or 16-bits), bit ordering (MSB first / LSB first), clock polarity and phase as well as bit rate.

### eSi-UART

The eSi-UART core can be used to implement asynchronous serial communications. It is ideally suited for implementing RS232 or ISO7816-3 for smartcard based connectivity. It supports a wide range of software configurable UART settings including 7 or 8 bit data, 1 or 2 stop bits and parity. The module supports ISO7816-3 modes T=0 and T=1 with hardware NACK and retry functionality.

### eSi-EMAC

The eSi-EMAC core implements an Ethernet Media Access Controller (MAC), providing access to 10/100Mbps Ethernet networks. It is a highly compact design featuring low gate count and low power making it ideally suited for providing network connectivity to 16 or 32-bit MCUs supporting an AMBA APB Bus or similar interface.

### eSi-USB

Fully certified peripheral device controller with software stack is available supporting USB2.0 either Full/High Speed or High/Slow Speed operations. The number of end-point are configurable as well as the option for a dedicated AHB DMA controller. A low gate-count and remote wake-up functionality makes it ideal for low-power applications.

### eSi-GPIO

The eSi-GPIO is a fully featured GPIO controller, the IP provides bi-directional inputs and outputs, plus optional level/edge detection of each input for generating interrupts and pull-up/down control logic.

### eSi-PS/2

The eSi-PS/2 is a PS/2 host interface to communicate with devices such as keyboards and mice.

### eSi-RTC

The eSi-RTC implementation of a real-time clock (RTC) it provides time, calendar, calendar alarm and periodic alarm functionality.

### eSi-Timer

The eSi-Timer is a software programmable multi-function timer/counter used for system timing functions.

### eSi-PWM

The eSi-PWM is a pulse width modulation waveform generator. Features include a configurable number of PWM channels, runtime programmable duty cycle from 0% to 100% and configurable period.

### eSi-MultiChannelTimer

The eSi-MultichannelTimer is a low gate count multichannel timer. It has the following features; configurable number of channels, counter width and single-shot or continuous mode of operation.

### eSi-Watchdog

The eSi-Watchdog core can be used to generate an interrupt if a keep-alive sequence isn't written to its control registers at a regular interval. This would typically be used to determine whether a program is running correctly, on the assumption that a program that has crashed would not write the correct sequence. The interrupt output would typically drive either the reset or non-maskable interrupt on the MCU, to restart the program.

### eSi-FIR

The eSi-FIR core can be used to implement general purpose filtering of an external data source. The coefficients are programmable with no restrictions on symmetry. The core supports a time-shared input source for compatibility with multi-channel ADCs. The filter output can be decimated to reduce the data rate.

### eSi-SMI

The eSi-SMI core provides a static memory interface, allowing access to off-chip RAM, ROM and FLASH memory devices. It supports a configurable number of data (8/16/32) and address pins and configurable number of banks (1-8). Each bank has programmable settings, including: data width, wait states, write-protect and privilege-level.

### eSi-DMA

The eSi-DMA core can be used to implement memory-to-memory, memory-to-peripheral, peripheral-to-memory and peripheral-to-peripheral block data transfers.

It supports a configurable number of channels and number of peripherals and a programmable byte count, access size, burst length and addressing (incrementing / fixed). The design supports an AMBA 3 AHB-lite slave interface for control register access and an AMBA 3 AHB-lite master interface for data transfers.

### About EnSilica

EnSilica is an established company with many years' experience providing high quality front-end IC design services to customers undertaking FPGA and ASIC designs. We have an impressive record of success working across many market segments with particular expertise in multimedia

and communication applications. Our customers range from start-ups to blue-chip companies. EnSilica also offer a portfolio of IP, including a highly configurable 16/32 bit embedded processor called eSi-RISC and the eSi-Comms range of communications IP.

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