eASIC and EnSilica Announce 16-bit and 32-bit Soft Processors for
eASIC Nextreme Devices

Santa Clara, CA – January 10, 2014 – eASIC® Corporation, a leading provider of Single
Mask Adaptable ASIC™ and EnSilica, a leading independent provider of IC design services
and IP today announced the immediate availability of 16-bit (eSi-1600) and 32-bit (eSi-3200)
soft processor cores. The eSi-1600 and the eSi-3200 are based on an EnSilica’s eSi-RISC
highly versatile microprocessor architecture that can be optimized by application through
extensive configuration options and custom instructions.

The eSi-RISC architecture provides the flexibility to define a range of hardware functions that
minimize silicon area. On–chip memory requirements are reduced by inter-mixed 16-bit and 32-
bit instructions, resulting in high code density without compromising performance. eSi-RISC
utilizes the industry standard GNU optimizing C/C++ compiler and Eclipse IDE for rapid
software development, and supports efficient debugging through a JTAG interface and
hardware breakpoints. The eSi-RISC architecture also supports instruction and data cache
options for both the 16 and 32-bit processor and a MMU, Floating Point Unit and DSP
extensions.

“EnSilica are delighted to partner with eASIC and make our IP available through eASIC’s eZ-IP
Alliance Program” said Philip Faulkner, Director of Projects at EnSilica. “The combination of our
low cost, flexible, high performance processors and the fast design and turnaround time of
eASIC’s single mask ASIC devices enables customers to overcome the challenge of software
versus hardware partitioning across a wide range of applications. We look forward to continuing
to expand the portfolio of IP available under the program,” added Faulkner.

“The eSi-RISC processors make an ideal embedded solution for use on our single mask
adaptable ASIC devices,”” said Jasbinder Bhoot, vice president, worldwide marketing at eASIC
Corporation. “The small footprint coupled with the versatile configurations options provides a highly cost optimized and low power solution.

About eASIC

eASIC is a fabless semiconductor company offering breakthrough Single Mask Adaptable ASIC devices aimed at dramatically reducing the overall cost and time-to-production of customized semiconductor devices. Low-cost, high-performance and fast-turn ASIC and System-on-Chip designs are enabled through patented technology utilizing Via-layer customizable routing. This innovative fabric allows eASIC to offer a new generation of ASICs with significantly lower up-front costs than traditional ASICs.

Privately held eASIC Corporation is headquartered in Santa Clara, California. Investors include Khosla Ventures, Kleiner Perkins Caufield and Byers (KPCB), Crescendo Ventures, Seagate Technology (NASDAQ:STX) and Evergreen Partners. For more information on eASIC please visit www.easic.com.

About EnSilica

EnSilica is an established company with many years experience providing high quality IC design services and IP to customers undertaking IC developments. EnSilica has an impressive record of success working across many market segments with particular expertise in multimedia and communications applications. Customers range from start-ups to blue-chip companies. EnSilica can provide the full range of IC design services, from System Level Design, RTL coding and verification through to either a FPGA device or the physical design for structured ASIC or Standard Cell designs. EnSilica’s portfolio of IP, includes a highly configurable 16/32 bit embedded processor called eSi-RISC, the eSi-Comms range of communications IP, eSi-Connect range of processor peripherals and eSi-Crypto encryption IP. For further information about EnSilica, visit http://www.ensilica.com.

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