

Application Areas

- ▶ IEEE802.11a/n
- ▶ IEEE802.16 WiMax
- ▶ DVB, DAB

Features

The FFT IP consists of two separate variants:

- ▶ A complex valued IFFT/FFT.
- ▶ A real valued IFFT/FFT.

Three interfacing options are available:

- ▶ Avalon streaming I/O for simple connections.
- ▶ Avalon MM master I/O for SSRAM connection.
- ▶ Avalon MM burst master I/O for SDRAM connection.

The following feature table is common to each variant:

- ▶ Per transform selection of FFT size from 8 to 32768 points
- ▶ Per transform selection of FFT or IFFT.
- ▶ Efficient mixed radix 4/2 dragonfly for low cycle count.
- ▶ Block floating point scaling ensures excellent dynamic range.
- ▶ Data and twiddle bit widths are parameters, defaulting to 16.
- ▶ IEEE-754 convergent rounding after twiddle multiplications.
- ▶ 1/8 twiddle table storage for lowest ROM requirements.
- ▶ Dual-port internal memory for FFT temporary storage.
- ▶ Simple streaming data ports on input and output, both supporting backpressure to facilitate simple interfacing.
- ▶ Reference design for Altera Cyclone III FPGA available - porting to other FPGA vendor devices can be undertaken if required.

Specification

This complex valued FFT is an efficient implementation of the Decimation in Frequency (DIF) Cooley-Tukey FFT. Using low FPGA resources and a high clock speed, this design manages high throughput by careful design optimization. This results in an IP core well balanced between logic and throughput.

The real valued FFT uses a half size transform and a combining pass to generate the full transform. This means that the core has only half the scratch memory and cycle count of the complex valued transform. The twiddle table size cannot be reduced however because of the combining stage. For convenient integration into an Altera SOPC system, a variant of the transform is provided with

an Avalon MM slave register interface and Avalon MM master interfaces for the I/O. This means that the FFT can be connected to a wide variety of bursting slave ports, such as DDR(2/3/4) SDRAM, PCI etc, or to latency-aware pipelined slave ports such as SSRAM.

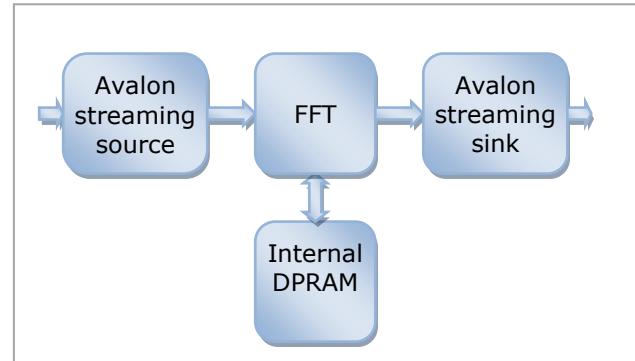


Figure 1: Streaming interface

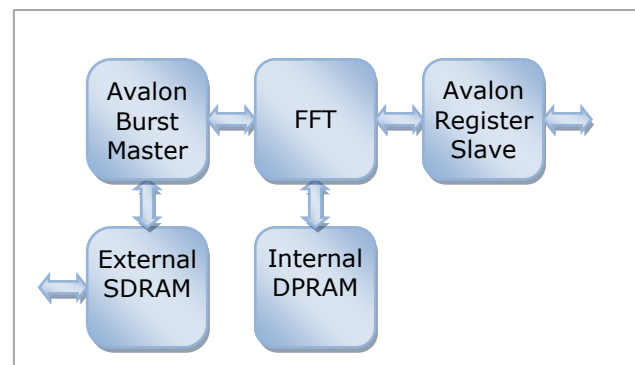


Figure 2: SDRAM burst interface

Resources

The following represent typical logic and memory resources are for an Altera Cyclone III 8192 point.

Variant	Logic ALUT	Memory (Bits)	M9K	9-bit mul	Fmax MHz
Streaming complex	1220	295,632	39	8	179
SDRAM Burst complex	1606	301,776	41	8	154
Streaming real	1703	164,544	23	8	186
SDRAM Burst real	2089	167,616	25	8	154

Ordering Guide

Please contact EnSilica with your requirements.

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