Application Areas

- IEEE802.11a/n
- IEEE802.16 WiMax
- DVB, DAB

Features

The Viterbi IP has the following features

- Constraint length 7.
- Generator polynomials g0 = 133_8 g1 = 171_8.
- Decoding 1 or 2 message bits per clock cycle.
- Block based traceback from best state.
- Optional trellis start state for packetised data.
- Optional trellis end state for packetised data.
- Low latency equal to 2.5x block length.
- Signed 6-bit soft decision (LLR) inputs for multilevel QAM decoding.
- De-puncturing support.
- Automatic normalization.
- Parameterisable soft core

Specification

This IP core is available in either normal or high throughput configurations. The normal configuration instances a single fully parallel stage, equivalent to 32 ACS units, decoding a single message bit per clock cycle. The high throughput version instances 2 fully parallel stages, equivalent to 64 ACS units, and an interleaved traceback memory architecture. This decoder produces 2 message bits per clock cycle, twice that of conventional Viterbi decoders.

The core can be used for streaming or packetised data applications. By using signed LLR input data it naturally supports de-puncturing by inserting zeros.

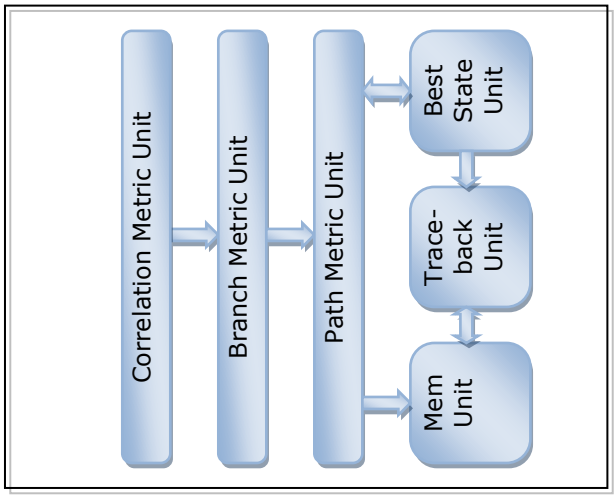
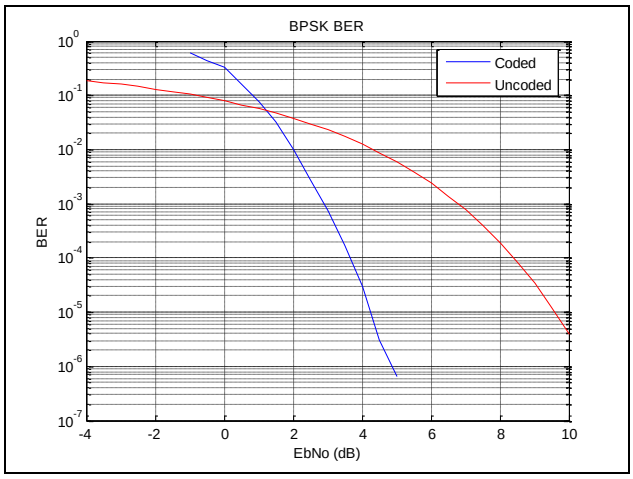


Figure 1: Architecture diagram

The traceback operates by performing a 64-bit block decode after a specified traceback length, and then moving forward a block length and repeating. In this way a high througput is maintained with low memory access requirements.

The traceback memory requirements are significantly lower than other Viterbi decoders, by implementing a novel architecture. For FPGA a dual-port memory architecture is appropriate, whereas for ASIC single port memories are used.



Resources

The following represent typical logic and memory resources for an Altera Stratix III. The logic resource usage is quite high because of the exceptional throughput that can be achieved, but the memory requirements are comparatively modest.

Variant	LUT	Mem Bits	Fmax MHz	ASIC gates	ASIC clock MHz
High thru, L=7, 3-bit soft, 64-bit traceback	4259	16K	120	25K	500
High thru L=7, 6-bit soft, 64-bit traceback	5645	16K 8x M9K	120	35K	500
Norm thru L=7, 6-bit soft, 64-bit traceback	3648	16K 4x M9K	120	25K	500

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