



eSi-7591 Viterbi Decoder

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2 Overview

The eSi-7591 core provides the control and data plane interfaces to a medium throughput Viterbi Decoder. It supports the following features:

- Constraint length 7.
- Generator polynomials $G0 = 133_8$ and $G1 = 171_8$.
- Configurable number of Radix-4 ACS units.
- Register exchange traceback from best state.
- Trellis termination state for packetised data.
- Trellis start state for packetised data.
- Low latency equal to traceback length.
- Fast traceback flush.
- 3-bit offset binary soft decision inputs.
- Erasure support for punctured code rates.
- Automatic normalization.
- No internal RAM.
- AMBA 3 AHB slave control interface.
- DMA control signals.

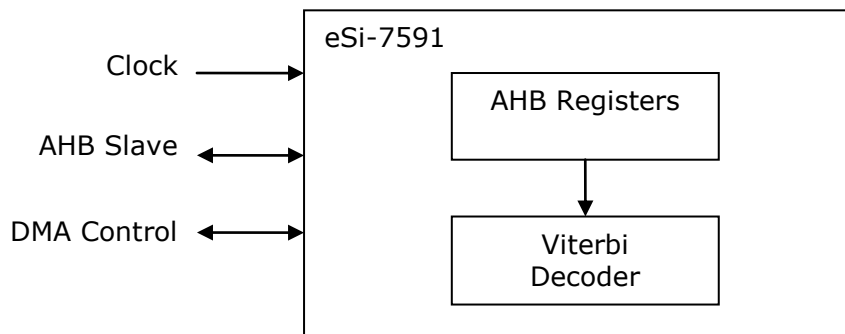


Figure 1: eSi-7591

The control logic handles the sequencing and control for decoding. The core is designed to operate independently through DMA I/O with handshake signals. It can also be operated in a block processing mode via software control, taking 32 symbol pair writes followed by a 32-bit decoded symbol read.

3 Hardware Interface

Module Name	esi_viterbi
HDL	Verilog 2001
Technology	Generic
Source Files	esi_viterbi.v, viterbi.v, acs2.v, acs2_1_stage.v, bsu.v, cntrl.v, emu.v, pmu.v, tbu.v, viterbi_include.v, mod_compare_include.v

Parameter	Range	Default	Description
TB_BLOCK	32-64	32	Traceback length
ACS_UNITS	1-16	4	Number of Radix-4 Add-Compare-Select units
CONSTRAINT_LENGTH	4,7	7	Constraint length
G0	-	133 ₈	Polynomial associated with symbol 0
G1	-	171 ₈	Polynomial associated with symbol 1

Table 1: Parameters

Port	Direction	Width	Description
s_hclk	Input	1	Clock
s_hresetn	Input	1	Reset, active-low
s_haddr	Input	32	Address
s_hburst	Input	3	Burst type
s_hmastlock	Input	1	Locked transfer
s_hprot	Input	4	Protection
s_hsize	Input	3	Size
s_htrans	Input	2	Transfer type
s_hwdata	Input	32	Write data
s_hwrite	Input	1	Write
s_hready_i	Input	1	Ready
s_hsel	Input	1	Select
s_hready_o	Output	1	Ready
s_hrdata	Output	32	Read data
s_hresp	Output	1	Response
tx_ready	Input	1	Indicates peripheral can accept new data
rx_ready	Input	1	Indicates peripheral has data to be read
tx_ack	Output	1	Acknowledges tx_ready after transfer complete
rx_ack	Output	1	Acknowledges rx_ready after transfer complete

Table 2: I/O Ports

For complete details of the AHB signals, please refer to the AMBA 3 AHB-Lite Protocol specifications available at <http://www.arm.com/products/solutions/AMBAHomePage.html>.

4 Software Interface

4.1 Register Map

The software register map is given below

Register	Address offset	Access	Description
control	0x00	W	Control register
status	0x04	R	Status register
data_in	0x08	R/W	Soft decision input register
data_out	0x0C	R/W	Decoded output bits register

Table 3: Register Map

4.1.1 Control Register

The control register contains a selection of flags that control the operation of the module.

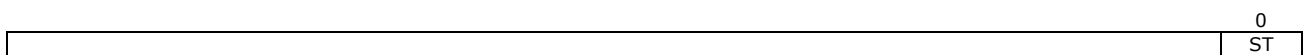


Figure 2: Format of the control register

Register	Values	Description
ST	0 – No effect 1 – Restart	Write '1' to start the decoder. This is a self clearing bit.

Table 4: Fields of the control register

4.1.2 Status Register

The status register contains a selection of flags that indicate the current status of the module.

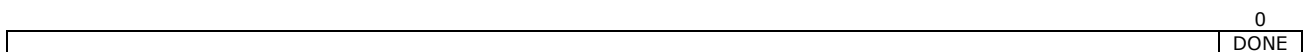


Figure 3: Format of the status register

Register	Values	Description
DONE	0 – Not complete 1 – Complete	Set to 1 when no more decoded bits to be read. Cleared after Viterbi is restarted.

Table 5: Fields of the status register

4.1.3 Data In Register

Holds the soft decision input data, puncture bits and end-of-packet flag. The decoder interface is setup such that 8-bit transfers can be used for unpunctured codes (E0 and E1 are read as '0'), however 16-bit transfers are necessary to support punctured codes in the receiver. The erasure bits E0 and E1 indicate to the decoder that these symbols were not sent across the medium, but were generated by the convolutional encoder.

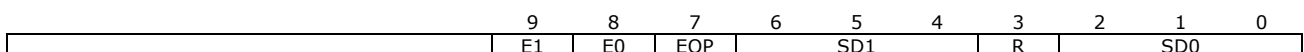


Figure 4: Format of the data_in register

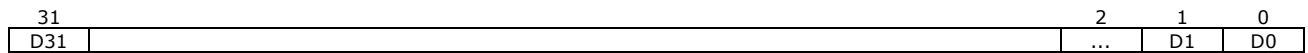
Register	Values	Description
SD0	0 – 7	Offset binary soft decision symbol associated with encoder output for polynomial G0.
R	-	Reserved
SD1	0 – 7	Offset binary soft decision symbol associated with encoder output for polynomial G1.

EOP	0 - Not last 1 - Last symbol pair	Set this to 1 to indicate the last symbol pair. The decoder will flush out the final decoded bits following this.
E0	0 - Not erased 1 - Erased	Set to 1 to erase SD0.
E1	0 - Not erased 1 - Erased	Set to 1 to erase SD1.

Table 6: Fields of the data_in register

4.1.4 Data Out Register

Holds 32-bits of decoded data after traceback.


Figure 5: Format of the data_out register

Register	Values	Description
D0...D31		Decoded output data, first bit in D0.

Table 7: Fields of the data_out register

5 Viterbi Operation

5.1 Soft decision format

In hard decision decoding the demodulator makes a firm (hard) decision on whether a one or zero was transmitted and provides no other information to the decoder about how reliable that decision is. For soft decision decoding the demodulator provides the decoder with some side information which is a measure of confidence for the decision. Soft coded data gives significantly better BER performance compared with hard coded data. Soft decision decoding offers approximately a 3dB increase in coding gain over hard-decision decoding. A choice of 3-bit soft decision width has negligible performance loss compared to floating point.

The soft decision is in offset binary format as shown in Table 8.

Offset binary	Interpretation
7	Most confident '1'
6	
5	
4	Least confident '1'
3	Least confident '0'
2	
1	
0	Most confident '0'

Table 8: Soft decision format

The metric units cost the incoming soft decision data using a Euclidean metric. The optimum demodulator would map the ideal BPSK symbol as shown below.

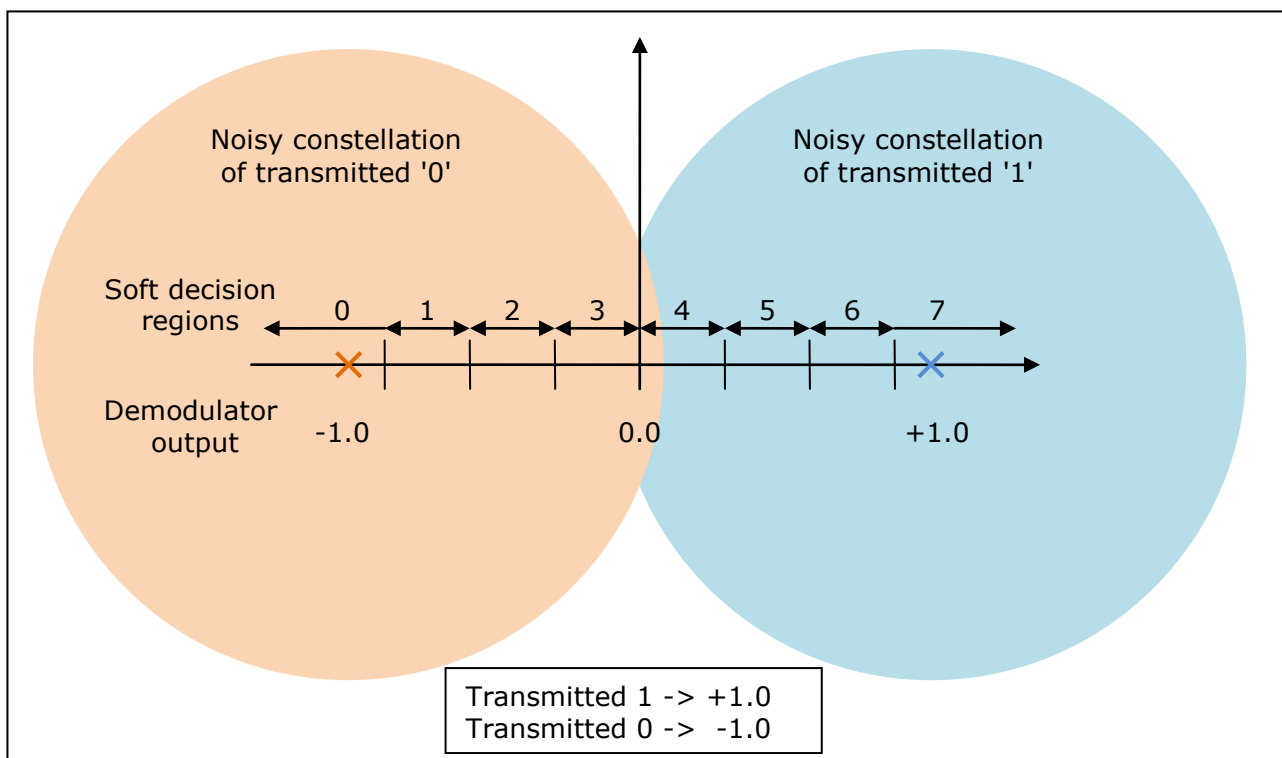


Figure 6: Example soft decision regions for BPSK demodulator

5.2 Interfacing

The Viterbi decoder is setup to operate efficiently as an AHB slave with DMA handshake signals for autonomous operation. For example

- The software should arrange soft decision data in 8-bit fields compatible with the `data_in` register. The final soft decision pair must have the `EOP` field set to 1. For punctured codes the software needs to use 16-bit fields to allow passing the erasure bits to the decoder.
- Set channel 0 of the DMA to write $N \times$ soft decision data pairs to the Viterbi `data_in` register.
- Set channel 1 of the DMA to read $N/32 \times$ 32-bit decoded data from the Viterbi `data_out` register.
- Set the `ST` bit in the `control` register to 1 to start DMA processing the data.
- The Viterbi finishes after the last decoded word is read from its interface.

To operate the Viterbi decoder using the register interface instead of DMA then the following sequence should be strictly followed.

- The software should arrange soft decision data in 8-bit fields compatible with the `data_in` register. The final soft decision pair must have the `EOP` field set to 1. For punctured codes the software needs to use 16-bit fields to allow passing the erasure bits to the decoder.
- Set the `ST` bit in the `control` register to 1 to start the Viterbi.
- (a) Write `TB_BLOCK` \times soft decision data pairs to the Viterbi `data_in` register.
- (b) Write 32 \times soft decision data pairs to the Viterbi `data_in` register.
- (c) Read 1 \times 32-bit decoded data from the Viterbi `data_out` register.
- (d) Repeat (b)-(c) write/read cycle above for soft decision input data.
- (e) Read final $\text{ceil}(\text{Tb_BLOCK}/32) \times$ 32-bit decoded data.
- The decode will naturally operate in this block processing mode.

5.3 Cycle count

The number of clock cycles required to decode each message bit is $(32/\text{ACS_UNITS})+1$, corresponding to 33, 17, 9, 5 and 3 clock cycles respectively. The ACS units and best state logic are efficiently timeshared.

5.4 Operation

The Viterbi decoder achieves an efficient implementation by timesharing Add-Compare-Select (ACS) units and best state logic to reduce the overall gatecount. Normalization is automatically handled internally so the accumulated path metrics cannot overflow.

The decoder is biased to start from state 0. Traceback is always from the best state, except after the end of packet where it starts from state 0, equivalent to terminating the trellis in this state. The traceback uses a register exchange algorithm for efficiency and results in very low latency.

The internal operation of the Viterbi decodes bits serially and these are then aggregated into a 32-bit word for the AHB interface. The traceback unit operates as follows. It waits for a block of up to `TB_BLOCK` survivor vectors. If it gets an end of frame (`EOP = true`) at any point in the first `TB_BLOCK` then it traces back from state 0 and outputs the decoded bits on `decoded_data` in `TB_BLOCK` cycles with `data_valid` true for valid bits. This is illustrated in Figure 7, where the only occurrence of `data_valid` is in a block at the end. If the end of frame occurs after `TB_BLOCK` then decoded bits are output on `decoded_data` and `data_valid` is set true for one clock pulse. At the end of packet the final decoded bit is output on `decoded_valid` with `data_valid` set true, and the remaining `TB_BLOCK` of the trellis are output in the next `TB_BLOCK` clock cycles. This is illustrated in Figure 8, where `data_valid` pulses occur after a

delay of TB_BLOCK processed symbols, and the flushed data occurs in a block at the end. Finally the done output is asserted during the last cycle. The done can be used to reset the decoder by connecting it to start.

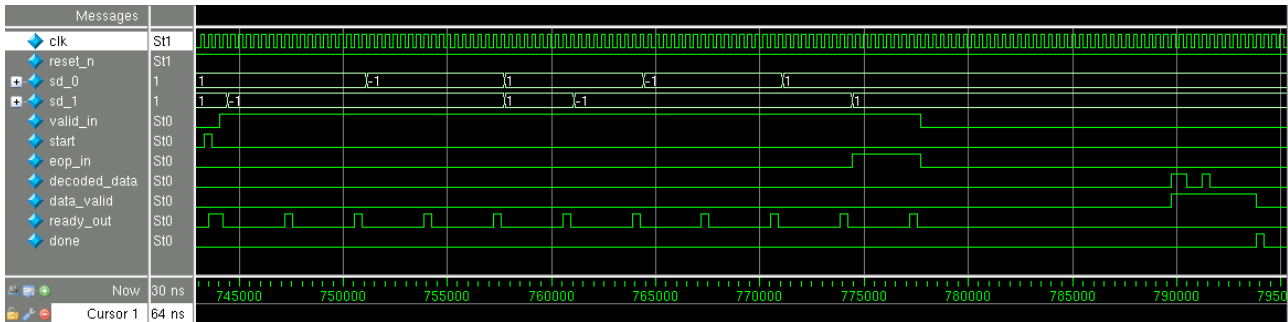


Figure 7: Interface detail when the sequence length is <= TB_BLOCK

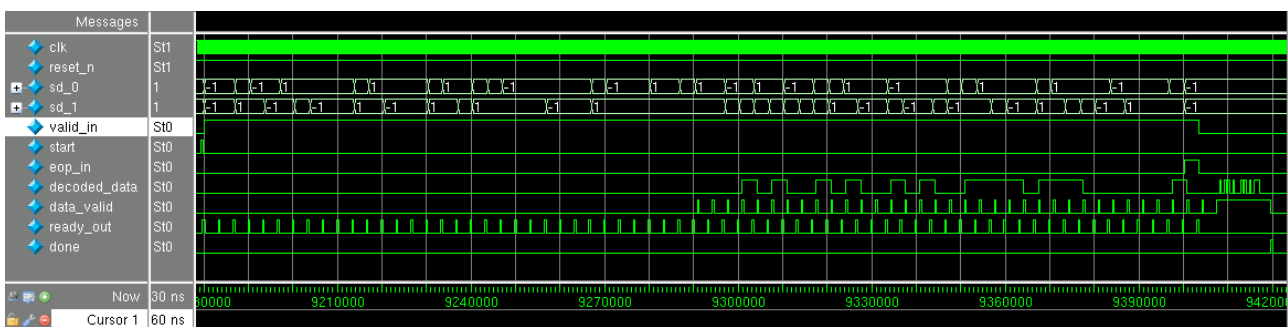


Figure 8: Interface detail when the sequence length is > TB_BLOCK

The input is double buffered to ensure that the next soft decision pair is pre-fetched for DMA transfers aiding efficiency. Similarly the output is double buffered so that the next 32-bit decode can progress while the DMA read is in progress.

5.5 Gatecount

The following gatecounts have been achieved, however they are for guidance only as the process technology node and clock frequency both have a significant impact.

L	Soft decision bits	Traceback	ACS units	Gates
7	3	32	1	34k
7	3	32	4	37k
7	3	40	1	39k
7	3	40	4	43k

Table 9: Typical gatecounts

5.6 Decoding performance

The test harness for this decoder encodes a continuous stream of bits into symbols adds noise and demaps the symbols according to Figure 6. The performance with varying soft decision bit width and a fixed 32-bit traceback is shown in Figure 9. It can be seen that the coding gain between 1-bit, or hard decision coding and 3-bit soft decision is about 3 dB. It can also be noted that the extra coding gain from having more bits in the soft decision is only around 0.1 dB at a BER of 1e-5. The coding gain measured at a BER of 1e-5 of this decoder is approximately 5dB over uncoded BPSK.

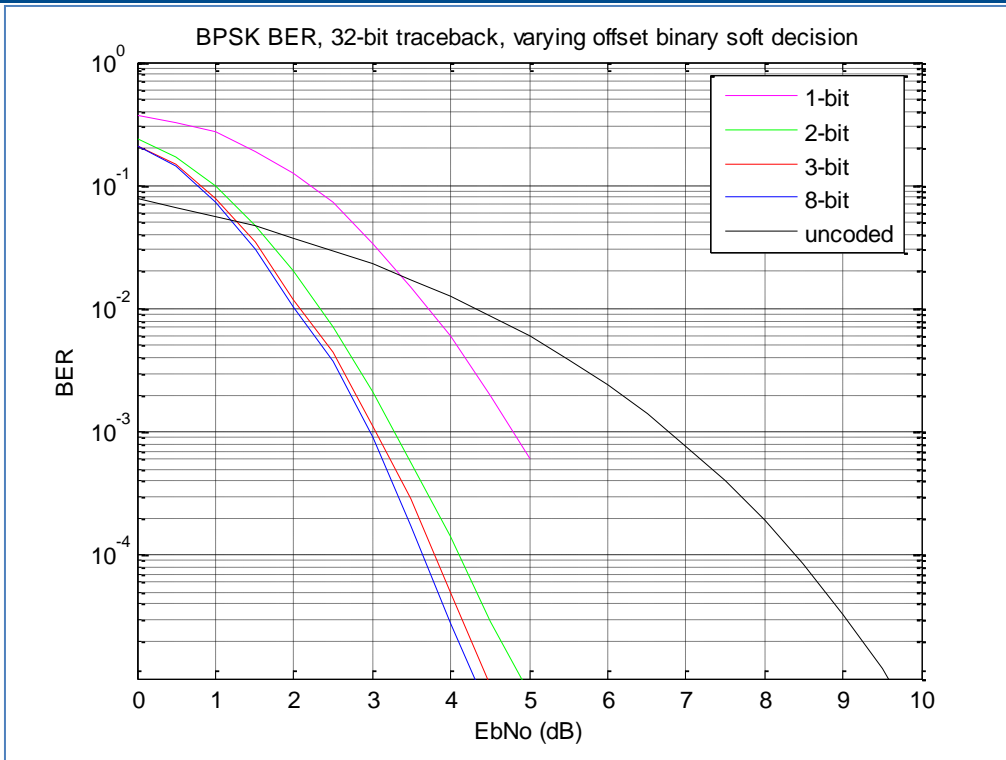


Figure 9: Performance with varying soft decision bit width

The effect of increasing traceback depth for an unpunctured code is shown in Figure 10. It can be seen that there is a 0.1 dB coding gain in increasing the traceback depth from 32 to 40. Increasing the depth further produces no extra coding gain. Note that for a highly punctured code, e.g. 7/8 code rate, the traceback depth should be increased to 64 which costs an extra 22k gates.

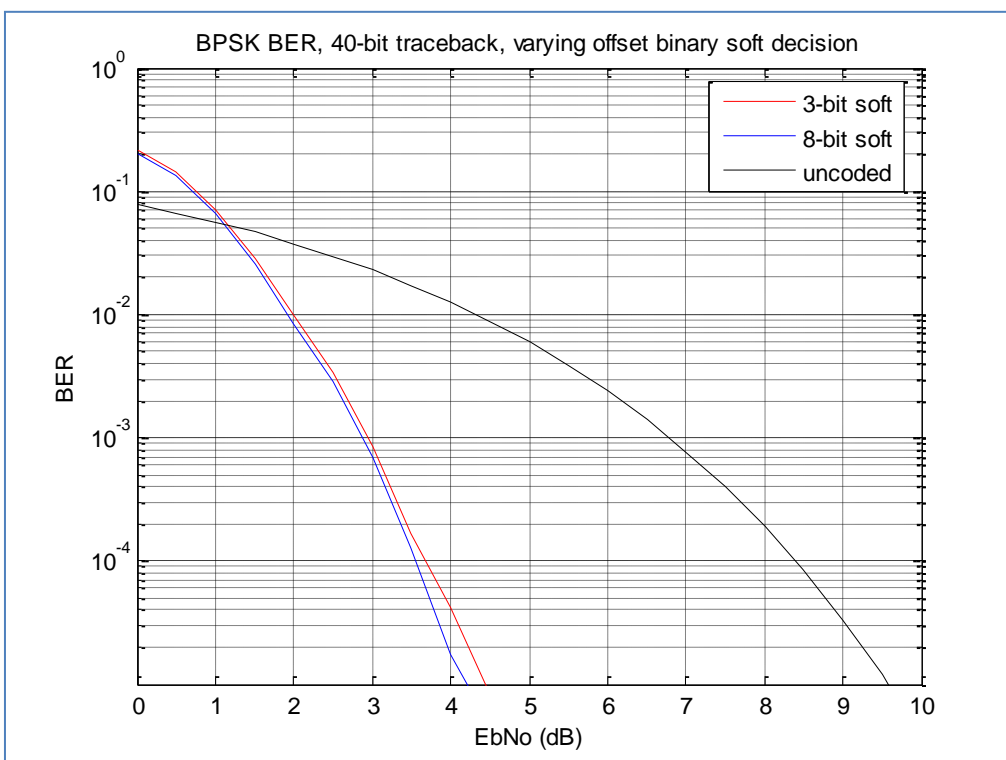


Figure 10: Performance with increased traceback depth