

Application Areas

- ▶ DVB using (204, 188)
- ▶ G.975/G.709 using (255, 239)
- ▶ CCDS using (255, 223)
- ▶ DSL
- ▶ 802.16-2004 WiMax using (255, 239)

Features

- ▶ Based on standard RS generating polynomials 285_8 or 207_8 .
- ▶ Available for FPGA or ASIC
- ▶ Supports shortening
- ▶ Supports erasures
- ▶ Run-time programmable codeword length

Specification

This is a Reed Solomon decoder capable of operating with shortened codewords. The basic mother rate is $(N,K) = (255,239)$ which has 16 parity bytes and can correct up to 8 corrupted bytes (up to 8 bits in a byte can be in error). The mother rate can be shortened to $N_MAX \leq 255$ but still retains the ability to correct up to 8 bytes in error. The decoder only outputs K bytes per N bytes in, and these are in natural order. It has enough memory to operate continuously with one byte per clock cycle on its input, leading to a net rate of $8 \cdot CLK$ bps of coded data. The codeword length is programmable at run-time.

The decoding is performed by first computing the Syndrome, and at the same time storing the input bytes in a memory. The syndrome is the sum of the parity check rows for all the error positions. To find the error positions and magnitudes involves solving a set of non-linear equations.

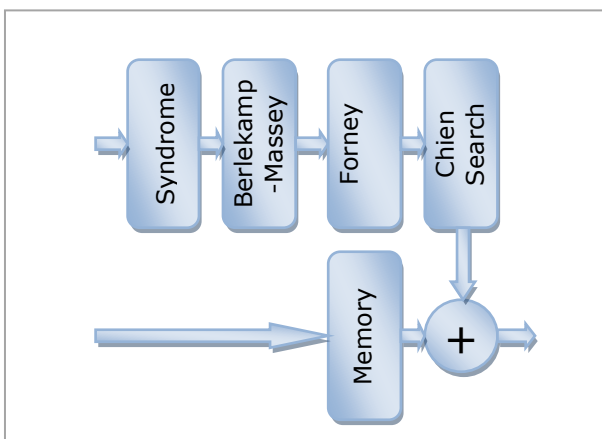


Figure 1: Block diagram

The Peterson-Gorenstein-Zierler algorithm performs this efficiently once the error locator polynomial can be found since the roots of this are at the inverse error positions. The process of determining the error locator polynomial and order is carried out by the Berlekamp-Massey algorithm.

The Chien search algorithm then substitutes all field elements to determine the roots and therefore the error locations. The error magnitudes are found from Forney's algorithm which determines the coefficients of an error evaluator polynomial.

The symbols are read out from the memory in natural order, corrected if in error, and output.

Benefits

The EnSilica Reed Solomon implementation is efficient and flexible; suitable for both ASIC and FPGA implementation. It benefits from simple dataflow I/O handshaking with backpressure to allow easy interfacing to the rest of the system. This decoder can achieve a throughput approaching $8 \cdot CLK$ bps.

Compared to other implementations this uses significantly less memory, only 6K bits, preferring to do calculations in logic rather than storing tables. For this reason the core is suitable in applications where on-chip memory resources are in short supply.

Resources

The following represent typical logic and memory resources are for an Altera Cyclone III.

Variant	Logic LUTs	M9K	9-bit mul	Fmax MHz
G.709	3400	2	0	110

About EnSilica

EnSilica is an established company with many years experience providing high quality IC design services to customers undertaking FPGA and ASIC designs. We have an impressive record of success working across many market segments with particular expertise in multimedia and communication applications. Our customers range from start-ups to blue-chip companies. EnSilica can provide the full range of front-end IC design services, from System Level Design, RTL coding and Verification through to either a FPGA device or the physical design interface (synthesis, STA and DFT) for ASIC designs. EnSilica also offer a portfolio of IP, including a highly configurable 16/32 bit embedded processor called eSi-RISC and the eSi-Comms range of communications IP.

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