



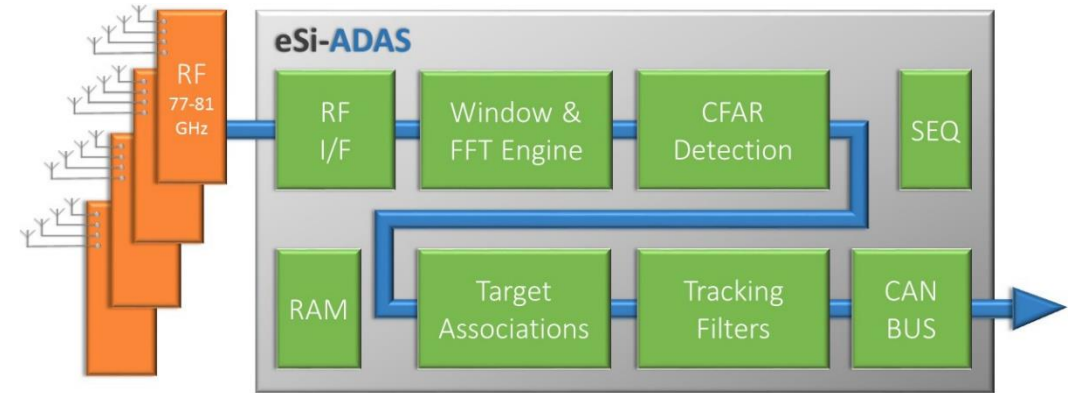
# eSi-ADAS

ADAS RADAR CO-PROCESSOR



# ADAS RADAR Co-Processing Solution

- Single chip eSi-ADAS RADAR DSP
- Highest levels of RADAR processing integration
- Lowest Power & Area
  - up to 20x lower than competitor solutions
- 10x target extraction and tracking of competitor solutions



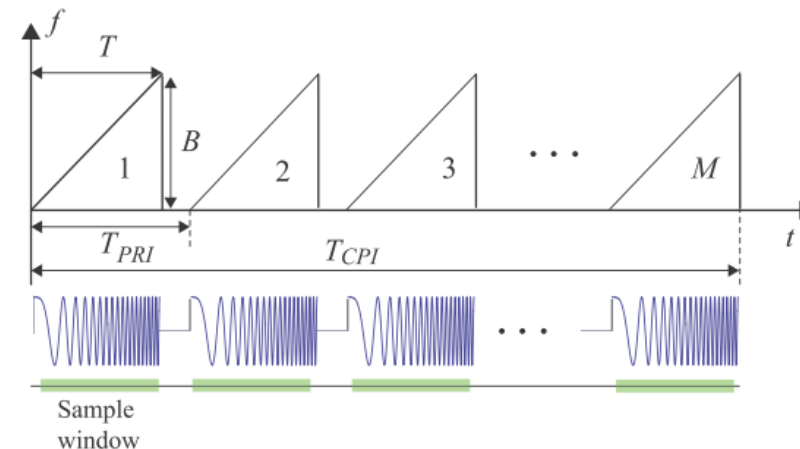
# Fast Chirp

## ■ Advantages

- Supports SRR, MRR and LRR with same processing
- Range and Doppler detection is independent
- Simple separation of Range and Doppler with same processing steps
- IF beat frequencies are out of  $1/f$  noise range
- IF beat frequencies are in low phase noise region of VCO
- Reduced power consumption from lower duty cycle

## ■ Disadvantages

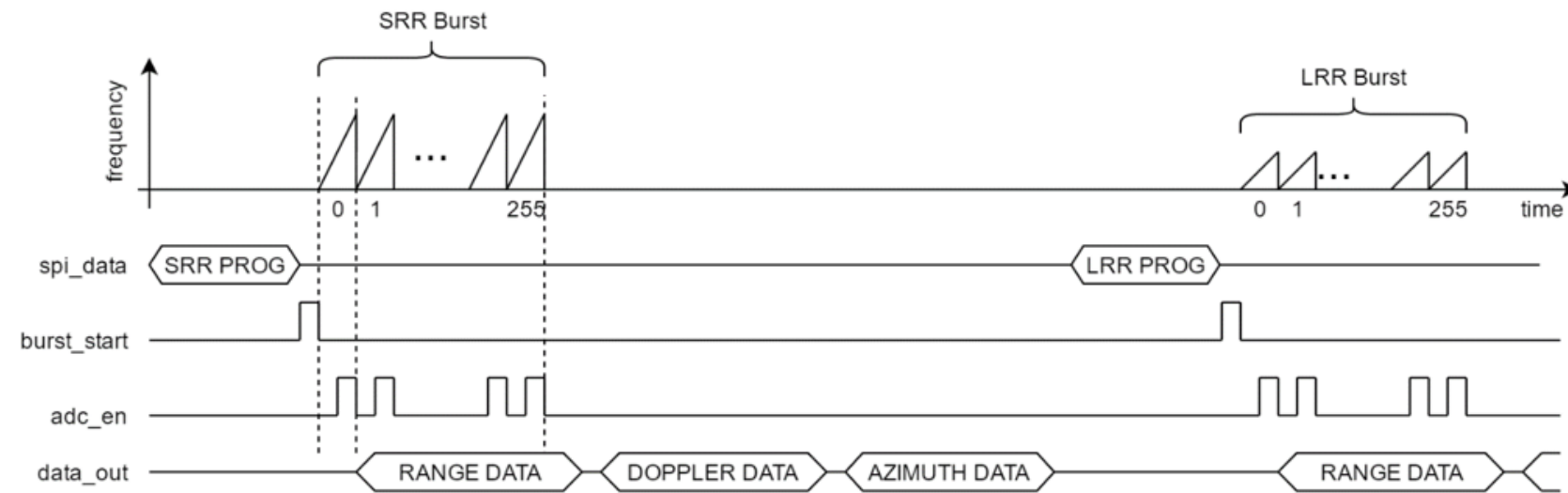
- Very high FFT processing rates
- Very large memory storage for data cube
- Complex VCO design
- High ADC specification



EnSilica Optimised Solution

# Fast Chirp Mode

- Up to 256 chirps in a measurement cycle
- 40 MHz sampling rate on each antenna
- Range, Doppler and Azimuth calculated separately for each mode
- Measurements from each mode are combined in the Tracking

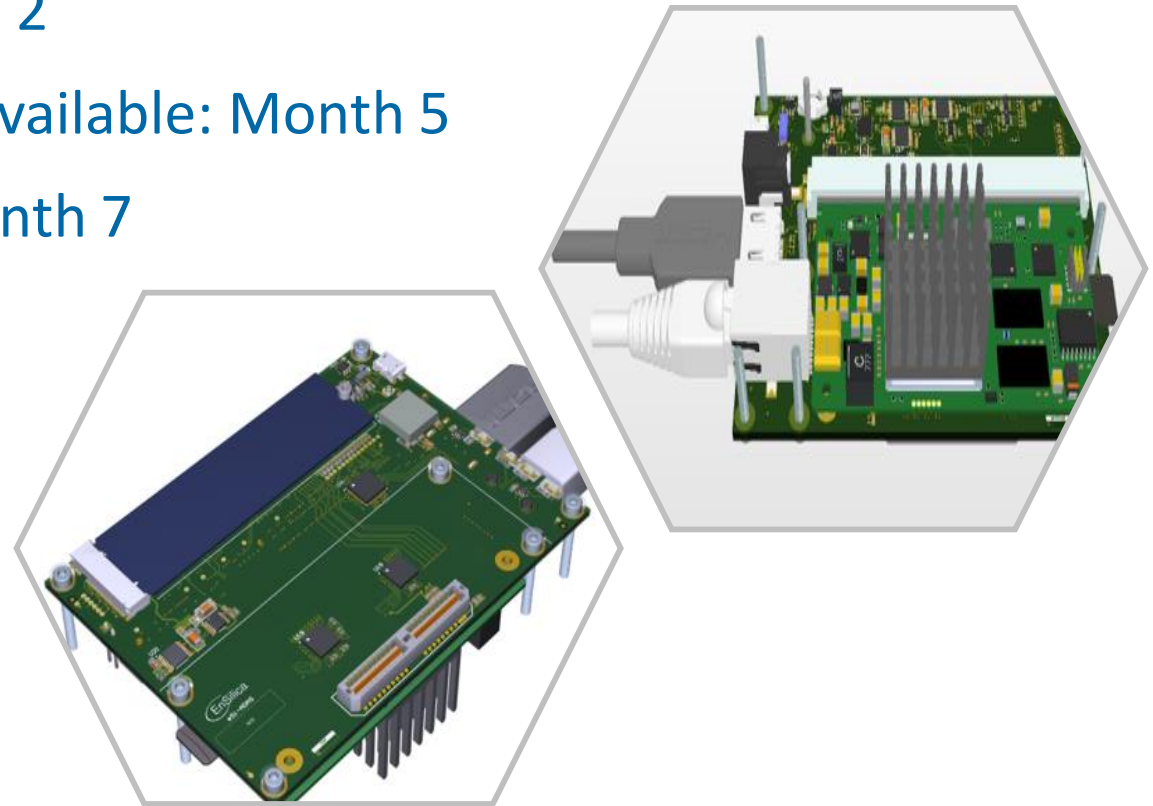


# ADAS Local DSP Features & Benefits

Feature	Benefit
Programmable all-hardware solution	Higher performance, lower power & reduced cost
No software to certify	Reduce automotive certification requirements
ASIL-B only	Lowest cost
Leading edge fast chirp DSP processing	TTM advantage over market leaders
Multichannel processing up to 12 antennas	Meets current & future customer demands
10x lower power consumption than competition	Low power, chip area & cost
20x lower RAM requirement than competition	Low power, chip area & cost
128 objects tracked in real-time	Significantly higher levels of tracking
Combined SRR and LRR object tracking	Leading edge performance
Minimal ECU management overhead	Can be controlled over simple serial interface
Low latency, target object list every 50ms	Rapid response to safety critical situations
Calculations can be accessed on fast bus	Processing chain can be easily customised

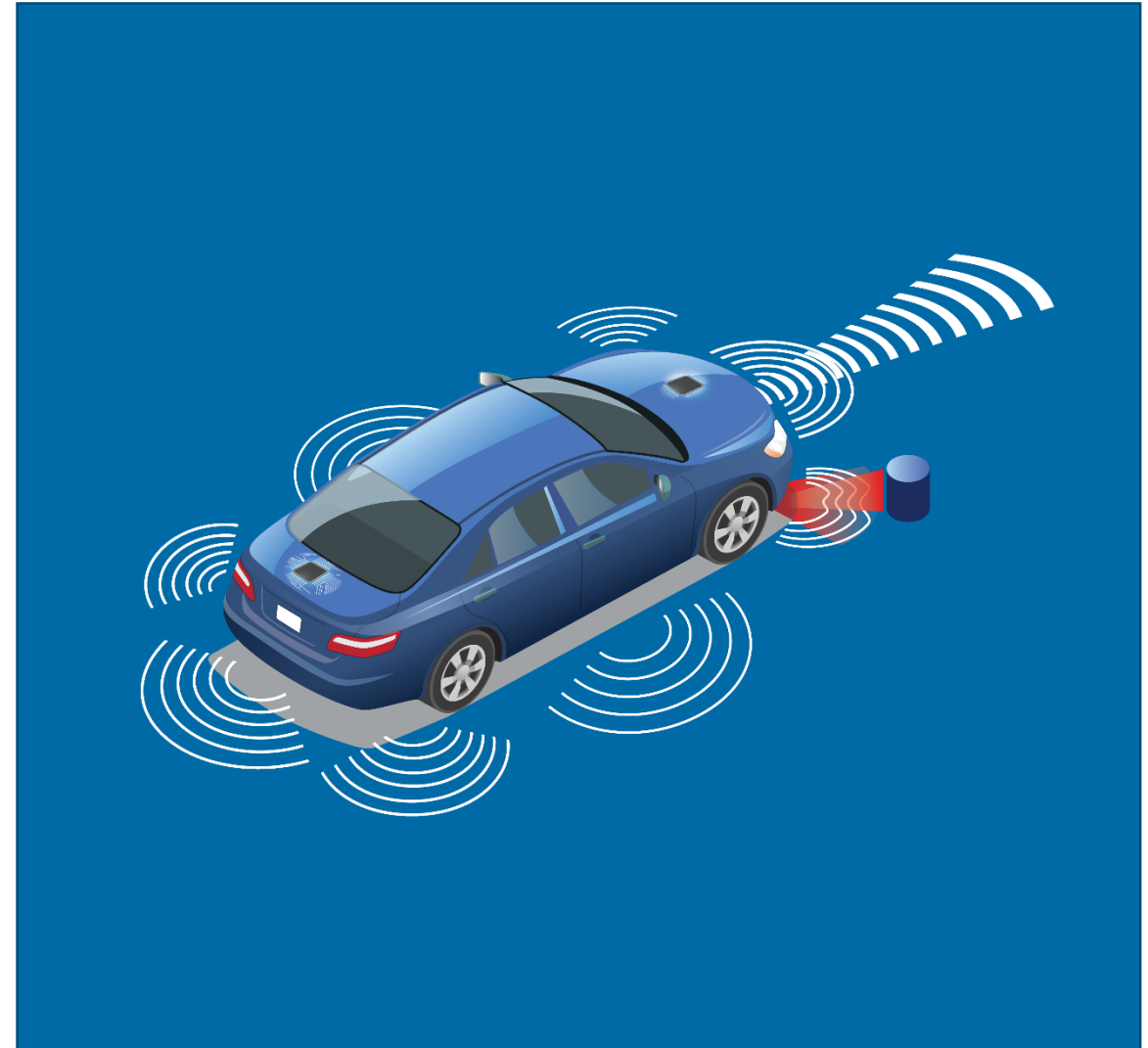
# Phase 1: FPGA Demonstrator

- Initial design & PCB manufacture: Now
- Enclosure manufacture: +1 month: Month 1
- Start Field Trials & Testing: Month 2
- Release 2 (Long Aperture Array) available: Month 5
- Code release 2 (3D) available: Month 7



# Conclusion

- eSi-ADAS is a maths co-processing engine
- Suitable for long aperture arrays and high sample rates
- Performs all the necessary DSP for plot and track extraction
- Lowest latency and power solution
- Low memory requirements from pipelined processing
- Free-up processors for track to object recognition and safety decisions



# Thank You

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